CLAIM AMENDMENTS

The following listing of claims replaces all prior listings and versions of claims in this application.

1. (Currently Amended) A processor comprising:

a plurality of registers;

circuitry configured to process a plurality of instructions associated with an instruction set including a plurality of branch and non-branch instructions, the plurality of instructions each having a multi-byte length, the plurality of instructions accessible at multi-byte aligned addresses;

common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate field in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions; and

wherein substantially all multi-byte aligned branch instructions are operable to access all ~~the~~ instructions at byte aligned addresses.

2. (Original) The processor of claim 1, wherein the plurality of instructions are accessed at word aligned addresses.

3. (Original) The processor of claim 1, wherein the plurality of instructions are accessed at half-word aligned addresses.

4. (Original) The processor of claim 1, wherein accessing the instructions comprises reading and writing the addresses.

5. (Original) The processor of claim 1, wherein branch instructions comprise branch and conditional branch instructions.

6. (Original) The processor of claim 1, wherein branch instructions comprise a branch offset and a current program counter value.

7. (Original) The processor of claim 1, wherein the units of branch offset and current program counter are in bytes.

8. (Original) The processor of claim 1, wherein the plurality of instructions are one word in length.

9-13. (Canceled)

14. (Currently Amended) A field programmable gate array, comprising:

a plurality of registers;

circuitry configured to process a plurality of branch and non-branch instructions associated with an instruction set, the plurality of branch instructions and non-branch instructions including an immediate field; and

common subcircuitry that performs a sign extension of an immediate field associated with one or more branch instructions and that performs a sign extension of said immediate field associated with one or more non-branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions, wherein the sign extension of the immediate field associated with one or more branch instructions is performed to determine a branch target address; and wherein each of the plurality of branch instructions and non-branch instructions has a multi-byte length and is operable to access all instructions at byte aligned addresses.

15. (Previously Presented) The field programmable gate array of claim 14, wherein the instruction set comprises a plurality of instructions.

16. (Previously Presented) The field programmable gate array of claim 15, wherein the plurality of instructions are accessed at half-word aligned addresses.

17. (Previously Presented) The field programmable gate array of claim 14, wherein branch instructions comprise branch and conditional branch instructions.

18. (Previously Presented) The field programmable gate array of claim 14, wherein common subcircuitry is used to handle the immediate field associated with the branch and non-branch instructions and wherein an immediate field value is maintained in units of bytes.

19. (Previously Presented) The field programmable gate array of claim 18, wherein common subcircuitry is used to perform sign-extensions of the immediate field associated with the branch and non-branch instructions.

20-30. (Canceled)

31. (Currently Amended) The processor of claim 1, wherein one of a primary or secondary component accesses memory of the ~~array~~ processor directly through ports without access through a system bus, and wherein the array does not comprises a system bus.

32. (Currently Amended) The field programmable gate array of claim 14, wherein one of a primary or secondary component accesses memory of the field programmable gate array directly through ports without access through a system bus, and wherein the array does not comprises a system bus.